

APPLICATIONS BRIEF 17 — REDUCING NOISE IN DESIGNS WITH ISD MULTILEVEL STORAGE DEVICES

Mixed analog digital systems can be susceptible to noise from the digital portions of the circuit getting into the analog portions.

Several common techniques can be used to minimize this such as:

- Separating grounds and supply lines until they return to the power supply.
- Avoiding the digital lines, particularly clocks, from running next to (or close to) low level audio lines.
- Bypassing of the supply lines.

Various techniques are practiced both inside and outside the IC devices used for mixed mode functions. On-chip the designers work very hard to keep the digital lines from influencing the analog circuits. Frequently there are separate pins for the digital and analog V_{CC} and ground connections.

Off chip, the PCB layout designers must work to maintain that effort in order to minimize any noise. The suggested external PCB techniques are detailed in this brief and in Figure 21. Depending upon the application, these can be very important. Using a differential microphone circuit helps reduce the pickup through the microphone AGC amplifier circuit. This amplifier can have as much as 24 dB of gain. A very small DC transient will be magnified to an obnoxious level if insufficient attention has been paid to the noise reduction techniques. The DC transients common to the ground and the V_{CC} are canceled by the common mode rejection ratio of the microphone amp connected in the differential configuration.

Applications not using the microphone amplifier are much less susceptible to noise. Here the audio input is provided to ANA IN pin through the recommended DC blocking capacitor. It is at a higher amplitude than that provided to the microphone amplifier and is not processed through an AGC amplifier stage. As a result the same amount of noise present on the supply lines is not amplified to same level as it would be through the AGC amp.

The above discussion has some application to the low level hiss present in all ISD devices. However, it is most applicable to the "hum" or "buzz" signal of 80 Hz (in the ISD1016A, ISD2532, ISD2560) that can sometimes be heard in the output. [In the ISD1110, ISD1020A, ISD2540, and the ISD2575 this is at a 64 Hz rate because of the lower sample rate.] This "buzz" comes from the rate at which the ISD devices write to the memory array. The ISD storage technique stores the incoming analog data serially in sample-and-hold capacitors. It then writes to "scans," or fractions of a row, in parallel. It is this parallel writing to many cells at a time that puts DC transients on the supply and ground lines. Because of these transients, it is advised in the ISD Applications Manual to run the ground trace from the digital V_{CC} pin bypass capacitor back to the power supply separately. This helps to reduce the noise present in the Analog Ground line that might influence the analog circuits. See "Good Audio Design Practices."

Many times it is possible to reduce the noise in an existing application merely by adding a single capacitor. Soldering a 0.1 μF capacitor across the bottom of the PCB between the V_{CCD} and V_{SSD} pins has been found to be effective in some cases. This can be used until a new PCB is designed to provide the suggested improvements. Another method to reduce the noise is to reduce the value of coupling and blocking capacitors in the audio path. Many telecom applications do not have any audio below 300 Hz. Choosing a 0.1 μF capacitor instead of a 1.0 μF , for example, between ANA IN and ANA OUT can reduce the amplitude of the "buzz" coupled into the array. Using smaller capacitor values on the speaker output lines can reduce any "buzz" that was recorded into the array. Reducing the capacitor values at the microphone amplifier pins from 0.22 μF (a previously recommended value in ISD schematics) to 0.1 μF is also very helpful (see Figure 19).

These and other standard PCB layout and bypassing practices ensure the continuing benefit of the ISD devices in application circuits.

Figure 19: Differential Electret Microphone Circuit (Preferred)

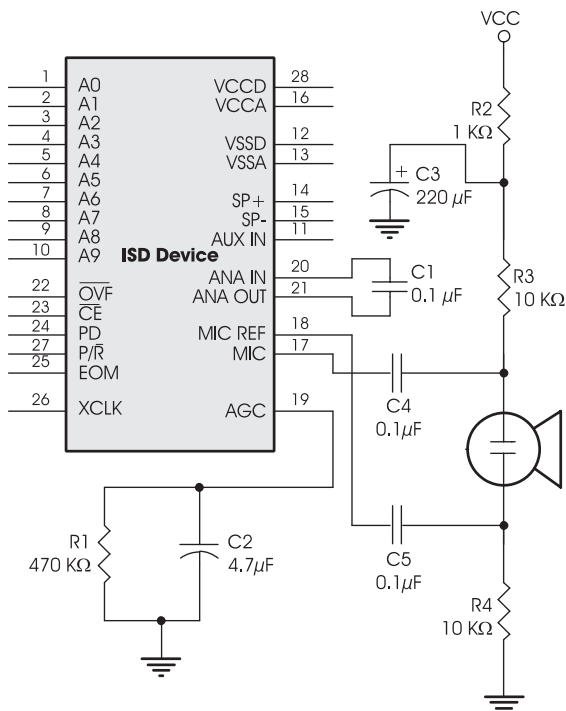


Figure 21 illustrates a suggested PCB layout to reduce noise from the digital circuitry affecting the analog circuitry. As one can see, the ground for the bypass capacitor from V_{CCD} is carried back to the supply ground on a separate trace from the analog grounds.

Figure 20: Single Ended Electret Microphone Circuit (obsolete)

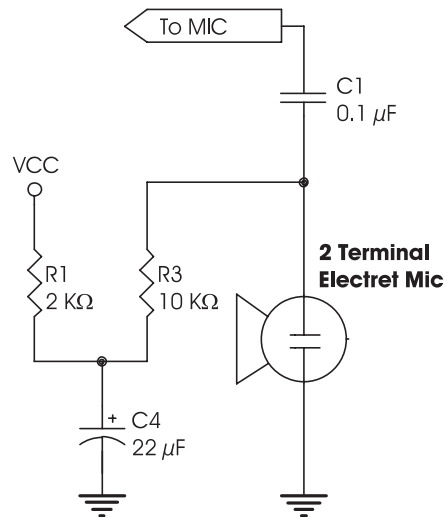
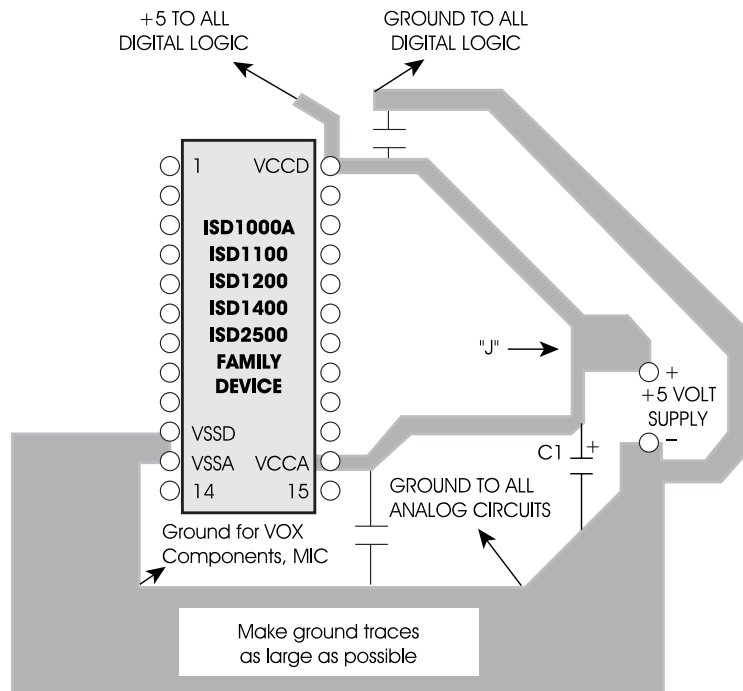


Figure 21: ISD Device Power and Ground Connections



NOTE: Address and control logic and audio connections are not shown. This drawing is for power connections only.