

Gate resistor installed Dual N-channel MOSFET

FC6B21100L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Low source-source ON Resistance: $R_{ss(on)}$ typ = 4.5 m Ω (V_{GS} = 4.5 V)
- CSP package:smallest & thinnest size
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 33

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS $T_a = 25\text{ }^{\circ}\text{C}$

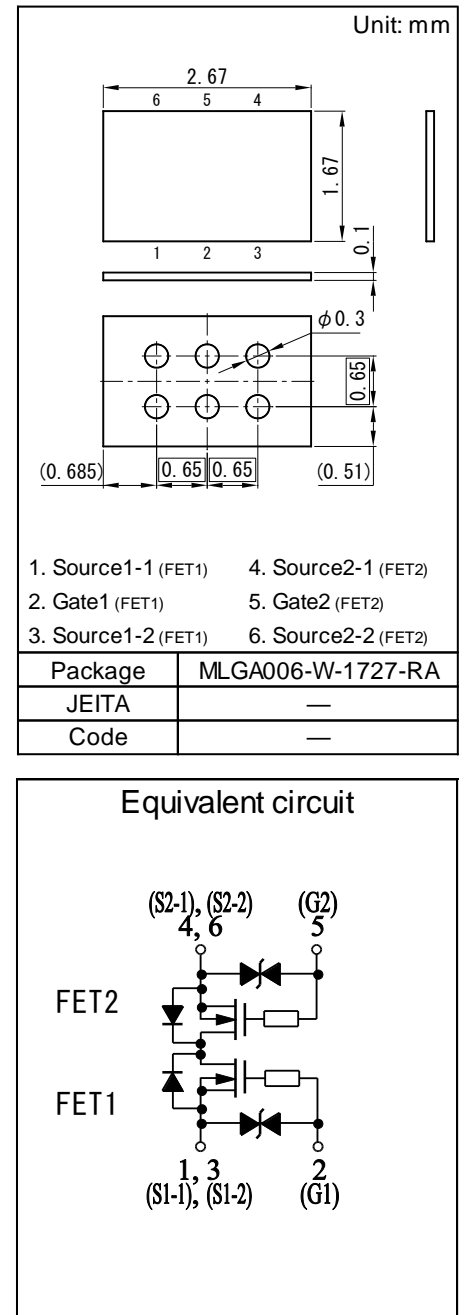
Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current (DC) ^{*1}	IS	8	A
Source Current (Pulsed) ^{*1,*2}	ISp	80	A
Total Power Dissipation ^{*1}	PD	0.45	W
Channel Temperature	Tch	150	$^{\circ}\text{C}$
Storage Temperature Range	Tstg	- 55 to + 150	$^{\circ}\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C}$

Parameter	Symbol	Rating	Unit
Thermal resistance (ch-a)	Rth(ch-a)	278	$^{\circ}\text{C} / \text{W}$

Note ^{*1} Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
using the minimum recommended pad size (36 μm Copper).

^{*2} $t = 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$.



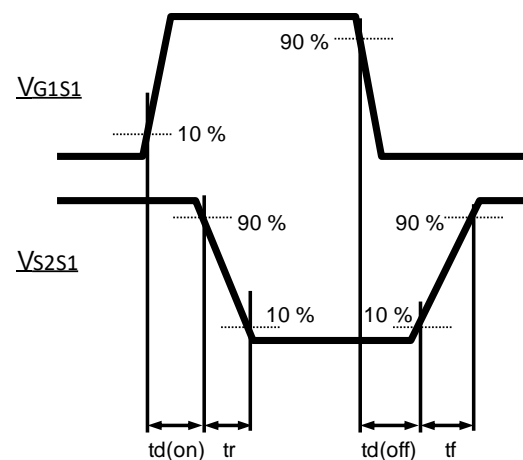
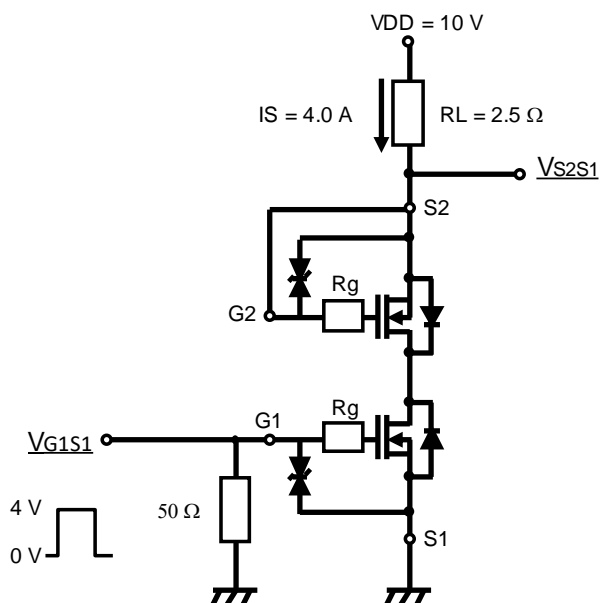
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	12			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
Gate-source Leakage Current	IGSS	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
		$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1	
Gate-source Threshold Voltage	V_{th}	$I_S = 1.0\text{ mA}$, $V_{SS} = 10\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 4.0\text{ A}$, $V_{GS} = 4.5\text{ V}$	3.4	4.5	5.7	m Ω
	RSS(on)2	$I_S = 4.0\text{ A}$, $V_{GS} = 3.8\text{ V}$	3.6	4.9	6.3	
	RSS(on)3	$I_S = 4.0\text{ A}$, $V_{GS} = 3.1\text{ V}$	4.0	5.5	7.8	
	RSS(on)4	$I_S = 4.0\text{ A}$, $V_{GS} = 2.5\text{ V}$	4.2	6.5	11.0	
Body Diode Forward Voltage	$V_{F(s-s)}$	$I_F = 8.0\text{ A}$, $V_{GS} = 0\text{ V}$		0.8	1.2	V
Input Capacitance ^{*1}	Ciss	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		4360		pF
Output Capacitance ^{*1}	Coss			720		
Reverse Transfer Capacitance ^{*1}	Crss			670		
Turn-on delay Time ^{*1,*2}	$t_{d(on)}$	$V_{DD} = 10\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$ $I_S = 4.0\text{ A}$		2.2		μs
Rise Time ^{*1,*2}	t_r			5.3		
Turn-off delay Time ^{*1,*2}	$t_{d(off)}$	$V_{DD} = 10\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$ $I_S = 4.0\text{ A}$		13.9		μs
Fall Time ^{*1,*2}	t_f			12.1		
Total Gate Charge ^{*1}	Qg	$V_{DD} = 10\text{ V}$ $V_{GS} = 0\text{ to }4\text{ V}$ $I_S = 8.0\text{ A}$		42		nC
Gate-source Charge ^{*1}	Qgs			14		
Gate-drain Charge ^{*1}	Qgd			13		

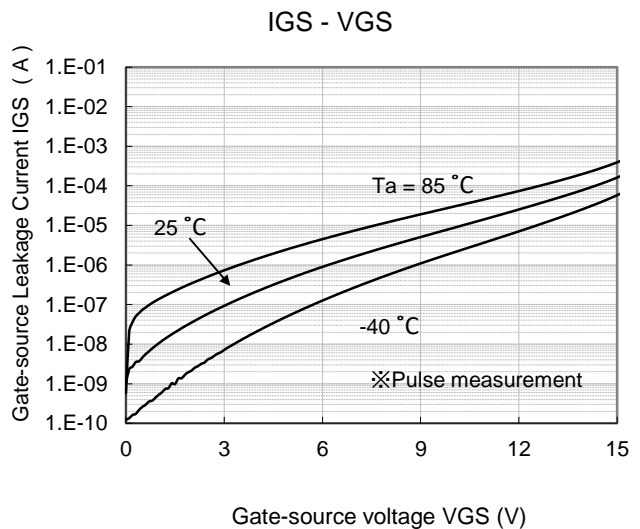
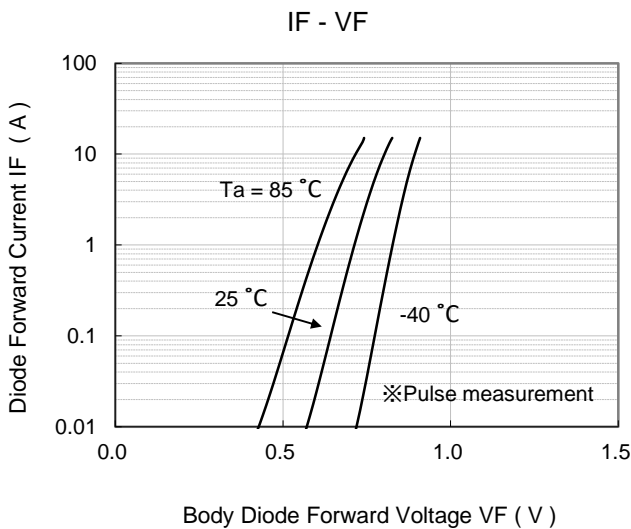
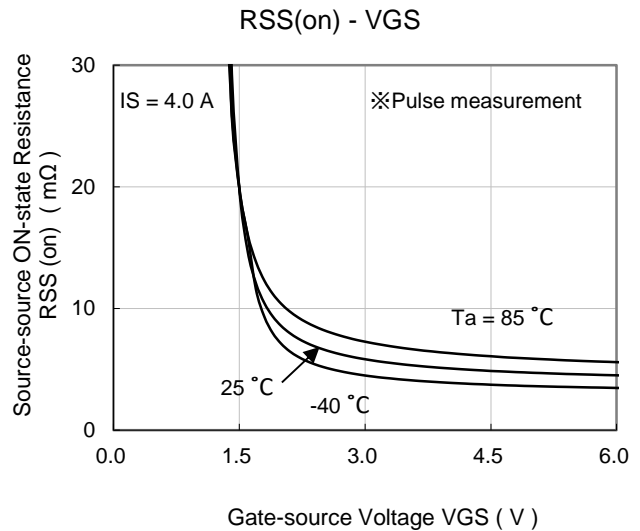
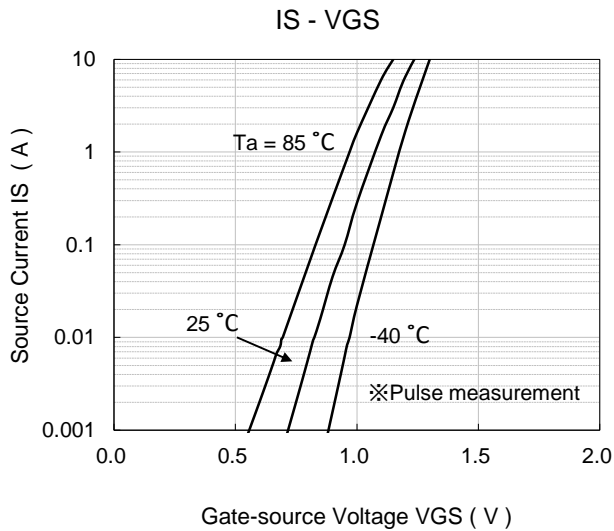
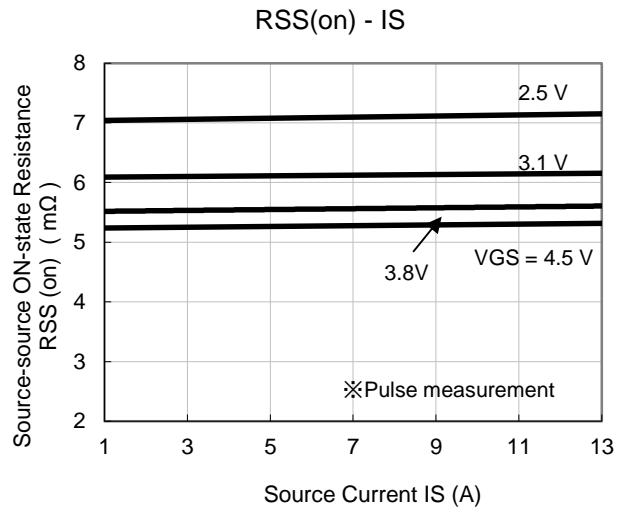
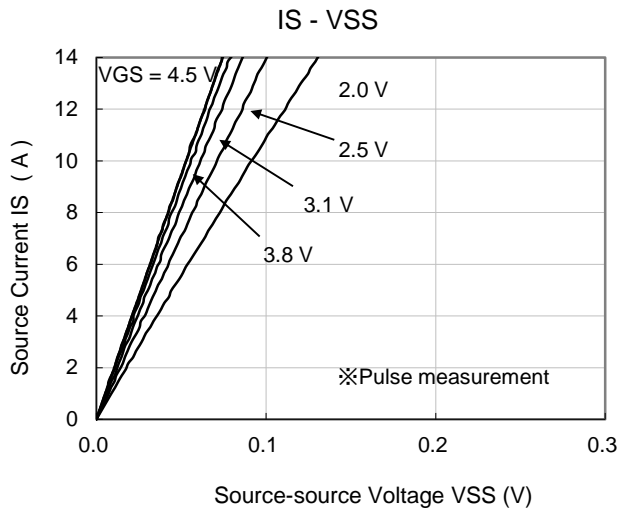
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

^{*1} Guaranteed by design

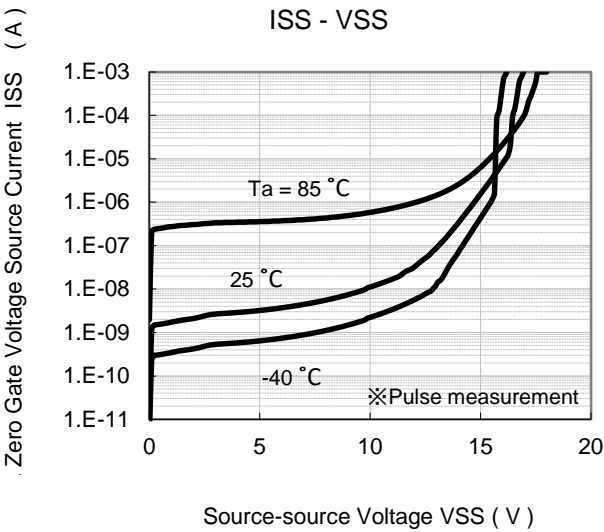
^{*2} Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



8. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)

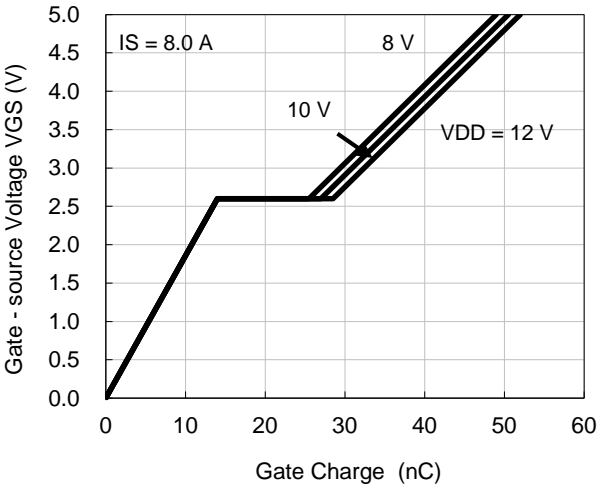


Destruction Current

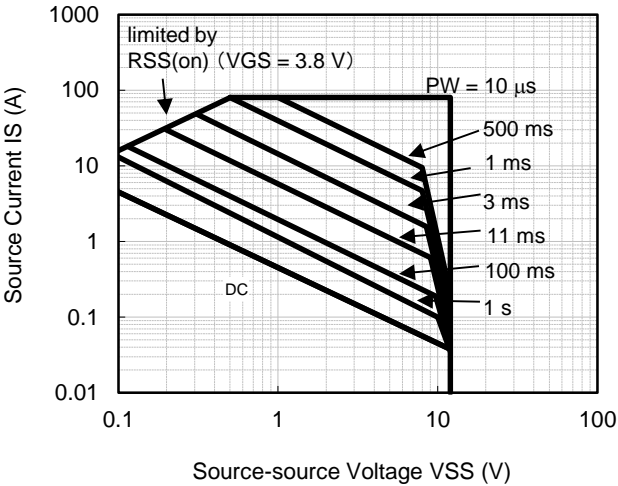
Parameter	Conditions	Result
Operation Test *1	VGS = 3.8 V, IS = 40 A, t = 3 ms	PASS
	VGS = 3.8 V, IS = 15 A, t = 11 ms	PASS
Destruction Current *1	VGS = 3.8 V, t = 300 μs	90 A
	VGS = 3.8 V, t = 10 ms	72 A
	VGS = 3.8 V, t = 20 ms	59 A
	VGS = 3.8 V, t = 50 ms	47 A
	VGS = 3.8 V, t = 100 ms	42 A
	VGS = 3.8 V, t = 200 ms	35 A

Ta = 25 °C,
Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm)
using the minimum recommended pad size (36μm Copper).

Dynamic Input/Output Characteristics

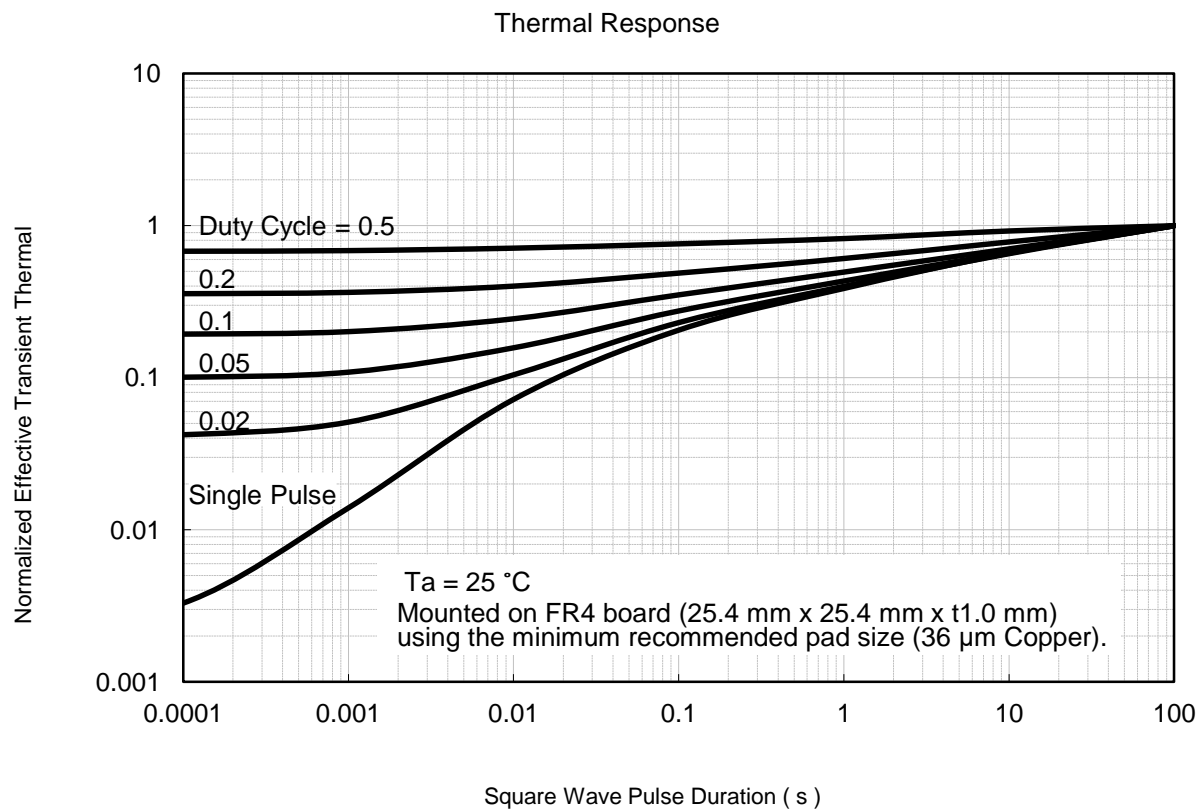
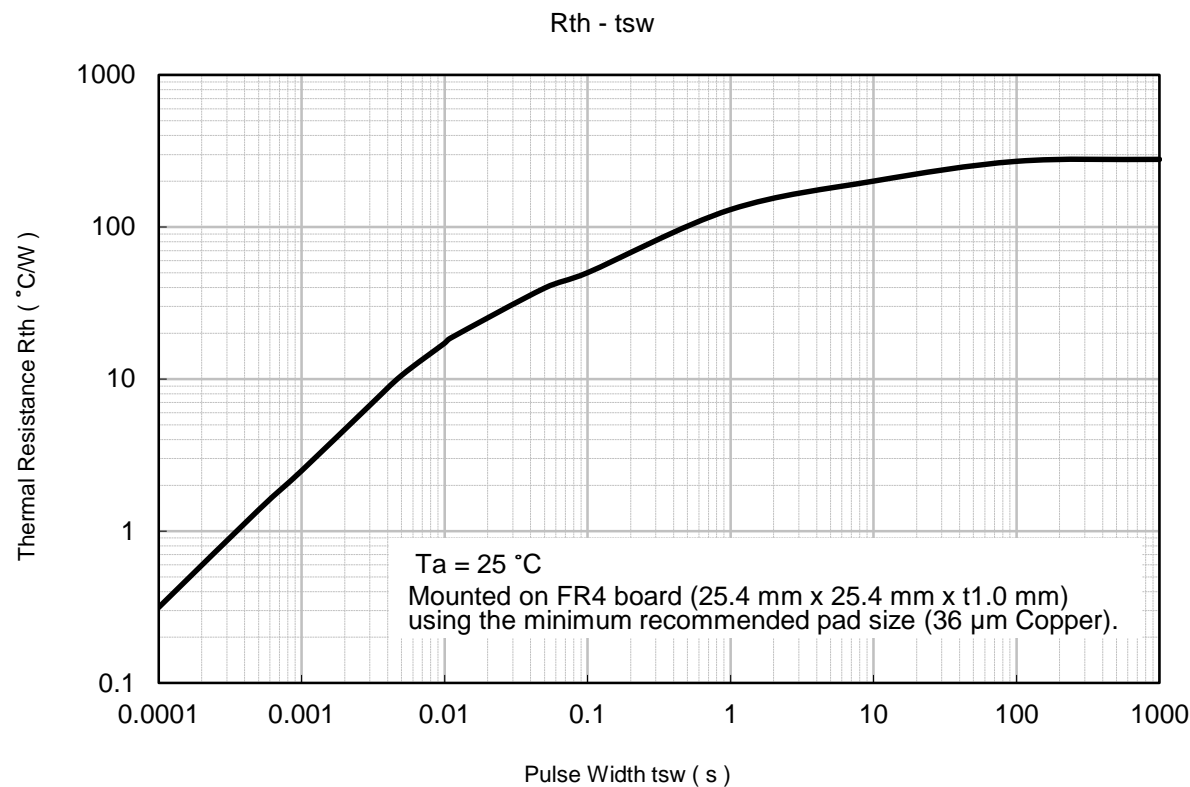


Safe Operating Area



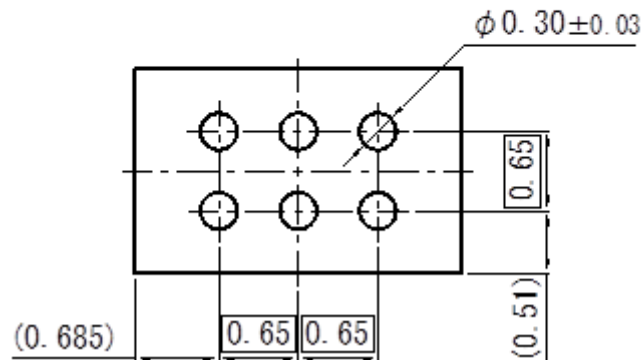
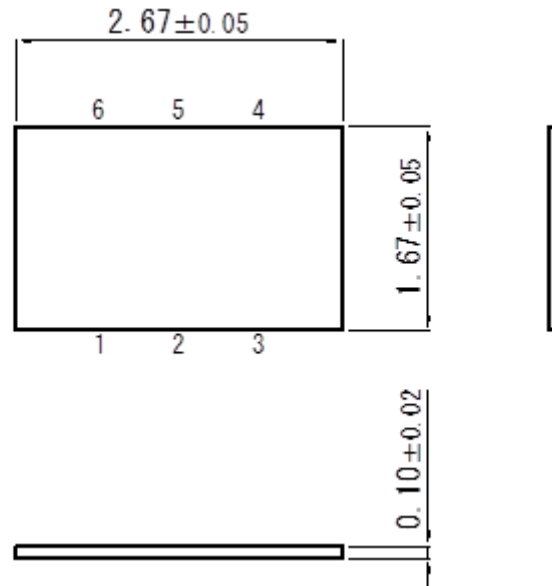
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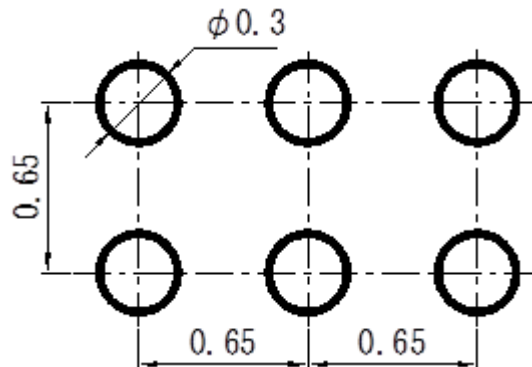
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.04.21	1.00	1. Initially issued.
2021.08.31	1.01	1. Added important notice in Land Pattern. 2. Added special attention and precautions notes.
2021.11.11	1.02	1. Changed document name from Product Standards to Datasheet.

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